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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,985	12/28/2001	Kevin X. Zhang	P11681	2439
7590	11/30/2004		EXAMINER	
John P. Ward BLAKELY, DOKOLOFF, TAYLOR & SAFMAN 12400 Wilshire Boulevard Seventh Floor Los Angeles, CA 90025			CONNOLLY, MARK A	
			ART UNIT	PAPER NUMBER
			2115	
DATE MAILED: 11/30/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/040,985	ZHANG ET AL.
	Examiner	Art Unit
	Mark Connolly	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 28 December 2001.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-18 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-18 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 28 December 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>1-15-04 &amp; 5-10-04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

1. Claims 1-18 have been presented for examination.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4, 6, 8-12, 15 and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by George et al [George] US Pat No 6785829.

4. Referring to claim 1, George teaches the processor comprising:

- a first local voltage regulator to be powered by a global voltage and to provide a first local voltage to power a first circuit of the processor [fig. 2, col. 4 lines 16-22].
- a second local voltage regulator to be powered by the global voltage and to provide a second local voltage to power a second circuit of the processor [col. 3 line 66-col. 4 line 2].

5. Referring to claim 2 George teaches that the first and second voltages are independently adjustable by the processor [fig. 2, col. 3 lines 38-50 and line 66-col. 4 line 2]. George shows that the processor can transmit a voltage identification code to the voltage regulator 240 via line 237. In addition, George also explicitly teaches that multiple independent variable supply voltages can be provided to the processor through multiple sub-variable voltage regulators in voltage regulator 240.

6. Referring to claim 4, George teaches setting a voltage to allow the processor to meet a timing requirement [abstract].

7. Referring to claim 5, George teaches that the voltage is adjusted based on a timing requirement. Therefore if a circuit is inactive, its timing requirement reduces therefore necessitating a decrease in voltage applied to the circuit. Therefore it is interpreted by the examiner that if a circuit is inactive, the Hall system reduces the voltage being applied to that circuit regardless of the current state of a second circuit and vice versa.

8. Referring to claim 6, George teaches a port for receiving a global voltage from an external voltage regulator [250 fig. 2].

9. Referring to claim 8, George teaches that a first circuit includes a processor core and a second circuit includes a cache [fig. 3].

10. Referring to claims 9 and 10, these are rejected on the same basis as set forth hereinabove. George teaches the processor and therefore teaches the system comprising the processor.

11. Referring to claim 11, George teaches adjusting the voltages if a sleep mode is desired [fig. 6A].

12. Referring to claims 12 and 14, these are rejected on the same basis as set forth hereinabove.

13. Referring to claims 15-18, these are rejected on the same basis as set forth hereinabove. George teaches the system and processor and therefore teaches the method performed by the system and processor.

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1, 2, 9 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hall et al [Hall] US Pat No 5787014.
16. Referring to claim 1, Hall teaches the processor comprising:
  - a. a first local voltage regulator to be powered by a global voltage and to provide a first local voltage to power a first circuit of the processor [fig. 1].
  - b. a second local voltage regulator to be powered by the global voltage and to provide a second local voltage to power a second circuit of the processor [fig. 1].
17. Referring to claim 2, Hall teaches that the first and second voltages are independently adjustable by the processor [fig. 1, Table I and col. 5 lines 7-17].
18. Referring to claims 9 and 15, these are rejected on the same basis as set forth hereinabove. Hall teaches the processor and therefore teaches the system including the processor and the method performed by the processor.

***Claim Rejections - 35 USC § 103***

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
20. Claims 3, 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hall as applied to claims 1, 2, 9 and 15 above.

21. Referring to claims 3, 7 and 13 although Hall teaches a processor controlling a voltage regulator, it is not explicitly taught that the voltage regulator include a digitized resistor or op-amp. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a digitized resistor or op-amp in the voltage regulators in the Hall system because Hall explicitly teaches that "any of a wide variety of voltage regulators can be used with the present invention" and voltage regulators with digitized resistors and op-amps are well known in the art.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly  
Examiner  
Art Unit 2115

  
THOMAS LEE  
EXAMINER  
TELEPHONE NUMBER 2115

mc  
November 20, 2004